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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/568,965	02/21/2006	Yasuhiro Maenishi	20060216A	8888
52349 7590 12/31/2007 WENDEROTH, LIND & PONACK L.L.P. 2033 K. STREET, NW SUITE 800 WASHINGTON, DC 20006			EXAMINER BAHTA, KIDEST	
			ART UNIT 2125	PAPER NUMBER
			MAIL DATE 12/31/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/568,965

Applicant(s)

MAENISHI ET AL.

Examiner

Kidest Bahta

Art Unit

2125

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>2/21/06</u> . | 6) <input type="checkbox"/> Other: ____. |

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP-A-1227711 (Matsushita Electric Industrial Co., LTD).

Regarding claims 1 and 13-16, Matsushita Electric Industrial discloses an optimization method for optimizing an order of component mounting in a component mounting system having a plurality of placement heads for mounting components on a board ([0084] "In this improved step repeat method, the order of mounting of electronic components is similar to that of the conventional step repeat method as shown in Fig. 7, where the mounting is carried out in the order of chip components -> SOPS -> QFPs as shown by arrows in Fig. 7. More specifically, as placement steps are shown sequentially in Fig. 8, the first steps include sucking up the chip component C1 to the first placement head 38a, the chip component C5 to the second placement head 38b, and the chip component C9 to the third placement head 38c by S-size suction nozzles, respectively, all simultaneously or each individually, moving the transfer head 28, and placing the chip C5, C9 onto the respective sub-boards in this order"), wherein a plurality of patterns having the same component placement structure is included in the board ([0056] "Fig. 7 is a view showing an order of placement by an improved step repeat method in an example of a multiple board composed of three sub-boards having an

identical pattern"), and the optimization method comprises an allocation step of allocating components, to each of the plurality of mounters, on a per pattern basis ([0084] same passage as above; Fig. 8 - all components of the first pattern ("SUB-BOARD" 1) are allocated to mounter ("PLACEMENT HEAD") 1, all of the second pattern to mounter 2, and all of the third pattern to mounter 3) The difference of claim 1 over the teaching of D1 is that where D1 disclosing having multiple "placement heads", claim 1 talks about multiple "mounters" instead.

However, to a skilled person it is known that "multiple mounters" is a general term encompassing independently moving mounters as well as multiple mounters that are fixed relatively to each other and operate with synchronous movement, such as "placement heads" in D1.

Therefore, choosing "multiple mounters" instead of "placement heads" is a choice among obvious design options that a skilled person would take upon circumstances, thus arriving at a solution as set out in claim 1 without using inventive activity. Choosing one option over the other does not achieve any surprising technical effect.

Regarding claims 2-12, 14-15, Matsushita Electric Industrial discloses,

2. The optimization method according to claim 1, further comprises a step of optimizing the order of component mounting for any one pattern among the plurality of patterns.

3. The optimization method according to claim 1, wherein the allocation step includes: a pattern number determination step of determining, from a total number of the patterns included in the board and a number of the mounters, a number of patterns to be allocated to each of the mounters so that the number of patterns is approximately even; and a pattern allocation step of allocating the determined number of patterns to any of the plurality of mounters for component mounting ([0078]-[0084]).

4. The optimization method according to claim 3, wherein the pattern number determination step includes: a step of calculating a quotient and a remainder by dividing the total number of the patterns included in the board by the number of mounters; a step of determining the quotient as the number of patterns to be allocated, in the case where the remainder is zero; and a step of i) determining a number, which is the quotient plus one, as the number of patterns to be allocated to the same number of mounters as the remainder, starting from the mounter in a process farthest upstream, and ii) determining the quotient as the number of patterns to be allocated to the rest of the mounters, in the case where the remainder is one or greater ([0084]-[0088]).

5. The optimization method according to claim 3, wherein the pattern number

determination step includes: a step of calculating a quotient and a remainder by dividing the total number of the patterns included in the board by the number of mounters; and a first allocation sub-step of determining the quotient as the number of patterns to be allocated to each of the mounters (Page 13, Table 1).

6. The optimization method according to claim 5, wherein the pattern number determination step further includes a second allocation sub-step of determining the remainder as the number of patterns to be commonly allocated to the plurality of mounters (Page 13, Table 1).

7. The optimization method according to claim 6, wherein in the second allocation sub-step, the number of patterns to be commonly allocated to the plurality of mounters is determined so that a time for component mounting for each of the mounters is approximately even ([0099]-[0100]).

8. The optimization method according to claim 6, wherein in the pattern allocation step, the patterns to be commonly allocated to the plurality of mounters are located in positions in the board on which components can be mounted by said plurality of mounters ([0084]-[0088]).

9. The optimization method according to claim 6, wherein the plurality of mounters is all of the mounters included in the component mounting system ([0084]).

10. The optimization method according to claim 3, wherein in the pattern allocation step, the determined number of patterns are allocated to each of the mounters, as the patterns on which components are to be mounted, so that borders between the determined number of patterns allocated to each of the mounters are set orthogonally to a direction in which the board moves ([0099]-[0100]).

11. The optimization method according to claim 1, further comprises a step of determining a position of the board during component mounting so that a moving distance, from a default position to the allocated pattern, of a head of each of the mounters is uniform for all of said mounters, the head being used for mounting components on the board ([0084]).

12. The optimization method according to claim 1, further comprises a step of determining placement positions of component cassettes used in component mounting so that a distance from the placement positions of the component cassettes to the allocated pattern, for each of the mounters is uniform for all of said mounters ([0084]).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kidest Bahta whose telephone number is 571-272-3737.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's


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supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application information Retrieval IPAIRI system. Status information for published applications may be obtained from either Private PMR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kidest Bahta



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